

## Patent Abstracts of Japan

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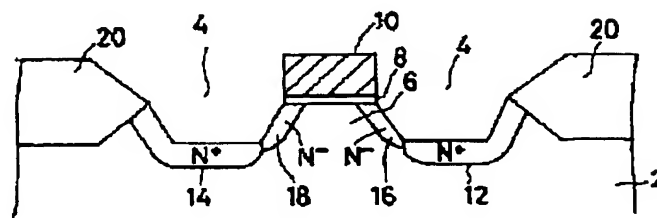
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APPLICANT : RICOH CO LTD;

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TITLE : SEMICONDUCTOR DEVICE AND  
MANUFACTURING METHOD  
THEREOF



ABSTRACT : PURPOSE: To lessen the short channel effect by suppressing the extension of a depletion layer within a MOS transistor in the structure wherein recessions are formed in a substrate while the substrate on a gate electrode forming part is raised.

CONSTITUTION: Recessions 4a are formed in source/drain regions in a P type silicon substrate 2 while a channel forming part becomes a raised part 6a on whose crest part a gate electrode 10 is formed through the intermediary of a gate oxide film 8. On the other hand, high doped source/drain regions 12, 14 are formed on the bottom parts of the recessions 4a while low doped source/drain regions 16, 18 are formed on the sides of the raised part 6a so as to form an LDD structured MOS transistor. Furthermore, a P type impurity diffused regions 26 in the same conductivity type as that of the substrate 2 but higher impurity concentration than that of the substrate 2 is formed in the deep position of the raised part 6a so as to suppress the extension of a depletion layer.

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